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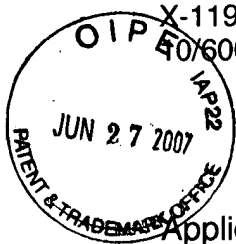
TRANSMITTAL FORM <small>(to be used for all correspondence after initial filing)</small>	Application / Conf. No.	10/600,848 / 7556
	Filing Date	June 19, 2003
	First Named Inventor	Jonathan B. Ballagh
	Examiner Name	Andre Pierre Louis
	Art Unit	2123
	Patent No.	
Mail Stop: AF	Attorney Docket Number	X-1192 US
Express Mail Receipt No.		
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X-1192 US
10/600,848

PATENT
Conf. No.:7556

IN THE UNITED STATES PATENT OFFICE

Applicants: Jonathan B. Ballagh et al.
Assignee: Xilinx, Inc.
Title: Clock Stabilization Detection For Hardware Simulation
Serial No.: 10/600,848 File Date: June 19, 2003
Examiner: Andre Pierre Louis Art Unit: 2123
Docket No.: X-1192 US Conf. No.: 7556

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AMENDMENT IN RESPONSE TO FINAL OFFICE ACTION

In response to the Final Office Action mailed from the Patent Office on May 3, 2007, please replace/substitute the following claims as indicated.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 9 of this paper.